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APPLICATION

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TITLE: METALLIZATION ARRANGEMENT FOR SEMICONDUCTOR STRUCTURE AND CORRESPONDING FABRICATION METHOD

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~~Description~~

Metallization arrangement for semiconductor structure and corresponding fabrication method

BACKGROUND

The present invention relates to a metallization arrangement for a semiconductor structure having a first substructure plane; a second metallization plane having a first and a second adjacent interconnect; a first intermediate dielectric for mutual electrical insulation of the first substructure plane and second metallization plane; and via holes filled with a conductive material in the first intermediate dielectric for connecting the first substructure plane and second metallization plane. The invention likewise relates to a corresponding fabrication method.

The term semiconductor structure is to be understood in the general sense and can therefore encompass both single-layered and multilayered structures with any desired semiconductor components. By way of example, the semiconductor structure is an integrated circuit for which the metallization arrangement provides internal or external wiring.

Figure 2 shows a diagrammatic illustration of a known metallization arrangement for a semiconductor structure.

In figure 2, 1 designates a semiconductor structure, for example an electrical circuit integrated in a silicon substrate, L1 designates a first liner layer made of silicon dioxide, M1 designates a first metallization plane, ILD designates an intermediate dielectric, V designates a via hole filled with a conductive material FM, L2 designates a second liner layer, M2 designates a second metallization layer, LBA designates a first interconnect, LBB designates a

second interconnect and O designates an interspace between the first and second interconnects LBA, LBB, and K designates critical locations of the structure.

In general, the aim of introducing the intermediate dielectric ILD having a low dielectric constant is to reduce the capacitive coupling of adjacent interconnects and thus improve the functional efficiency with the chip area unchanged. However, integrating the intermediate dielectric ILD having a low dielectric constant generally requires the provision of the liner layer L1 or L2, for example in the form of a silicon oxide liner or silicon nitride liner, for patterning the via holes V and as diffusion barrier (e.g. in the case of ALCu metallization).

The relatively high dielectric constant of such a liner layer L1 or L2 in the form of a silicon oxide liner or silicon nitride liner has an adverse effect, however, on the capacitive coupling of adjacent interconnects, for example LBA and LBB. Such critical locations in the known arrangement in accordance with figure 2 are designated by K.

SUMMARY

The present invention is based on the object of reducing the disturbing capacitive coupling.

According to the invention, this object is achieved by means of the semiconductor component specified in claim 1 and the fabrication method specified in claim 6.

According to the present invention, it is possible to considerably reduce disturbing capacitive coupling between adjacent interconnects of the second metallization plane.

The general idea underlying the present invention is that a liner layer made of a dielectric material is

provided under the second metallization plane, which liner layer is interrupted in the interspace between the first and second adjacent interconnects of the second metallization plane.

The subclaims contain advantageous developments and improvements of the semiconductor component specified in claim 1 and, respectively, of the fabrication method specified in claim 7.

In accordance with a preferred development, the first substructure plane is a first metallization plane.

In accordance with a further preferred development, the interspace between the first and second adjacent interconnects of the second metallization plane is filled with a second intermediate dielectric above the first intermediate dielectric. Thus, it is possible for a plurality of metallization layers with intervening dielectrics to be stacked one above the other.

In accordance with a further preferred development, the semiconductor structure has an electrical circuit integrated in a silicon substrate.

In accordance with a further preferred development, the liner layer is fabricated from silicon dioxide or silicon nitride.

In accordance with a further preferred development, the first and/or second metallization plane are/is fabricated from ALCu.

In accordance with a further preferred development, the patterning and interrupting are carried out in a common etching step. This requires merely the selection of a suitable etchant and/or of a suitable liner/metal combination. In comparison with the customary process,

there is then merely a need for a longer etching time, but not for an additional mask plane or an additional etching step.

In accordance with a further preferred development, the patterning is carried out in a first metal etching step and the interrupting is carried out in a second silicon dioxide etching step.

In accordance with a further preferred development, a hard mask or a resist mask, which is provided on the second metallization plane, is used for the patterning and interrupting processes.

An exemplary embodiment of the invention is illustrated in the drawings and explained in more detail in the description below.

Figures 1a-h show a diagrammatic illustration of the essential method steps for fabricating a metallization arrangement for a semiconductor structure as embodiment of the present invention; and

Figure 2 shows a diagrammatic illustration of a known metallization arrangement of a semiconductor structure.

In the figures, identical reference symbols designate identical or functionally identical elements.

DETAILED DESCRIPTION

Figures 1a-h show a diagrammatic illustration of the essential method steps for fabricating a metallization arrangement for a semiconductor structure as embodiment of the present invention.

As illustrated in figure 1a, first of all the first metallization layer M1 is deposited on the

semiconductor structure 1 and patterned. Afterward, an intermediate dielectric ILD1 is deposited over the whole area on the resulting structure. This intermediate dielectric ILD1 having a low dielectric constant is a carbon-containing SiO_2 layer, for example.

According to figure 1b, in a following process step, a liner layer L is applied to the resulting structure. In this respect, it should be noted that the dielectric constant of the liner layer L is greater than the dielectric constant of the intermediate dielectric ILD1.

The liner layer L and the intermediate dielectric ILD1 are then patterned by means of a standard photolithographic technique. This creates the via hole V, as illustrated in figure 1c.

In a further process step, as illustrated in figure 1d, the via hole V is then filled with the conductive filling material FM.

Afterward, or in the same process step, a second metallization layer M2 is then deposited, which leads to the structure shown in figure 1e.

A photoresist mask or, as in the present example, a hard mask made of silicon nitride, for example, is subsequently provided on the second metallization layer M2. Using the hard mask HM, the second metallization layer M2 is patterned into the interconnects LBA and LBB. This is illustrated in figure 1f.

Either in the same etching step or in an additional etching step using a different etching medium, the uncovered liner layer L is then etched away, with the result that the interspace O no longer contains any liner nor any metal. This is illustrated in figure 1g.

Consequently, the metal structure is transferred to the liner layer L made of silicon dioxide. Given suitable selection of the liner layer 6 and of the etching medium, this merely requires prolonging the known etching process for the metallization layer M2.

In accordance with the structure illustrated in figure 1h, the hard mask HM is then removed and a further intermediate dielectric layer ILD2 is deposited. Either a concluding passivation layer or a further third metallization layer, etc, can then be applied on said further intermediate dielectric ILD2.

As can clearly be seen from figure 1h, this type of process control results in the liner layer L made of silicon dioxide being removed wherever the metal layer M2 is also removed, with the result that the disturbing capacitive coupling effects are eliminated.

Although the present invention has been described above using a preferred exemplary embodiment, it is not restricted thereto but rather can be modified in diverse ways.

It goes without saying that the present invention can be applied to any desired semiconductor structures, in particular integrated circuits, and any desired basic semiconductor materials; in particular, it is possible to use any desired semiconductor materials or material sandwiches as substrates.

Although the first substructure plane is a metallization plane in the above example, it can also be a different plane, that is to say the invention can be applied to the bottommost metallization plane.